Arm Cortex-M0 Processor Datasheet

Datasheet

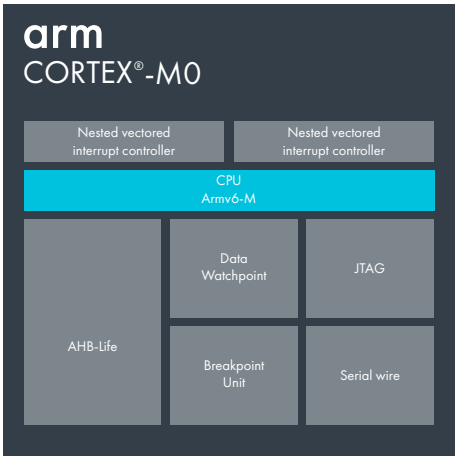


Figure 1:
Block diagram of the Cortex-M0 processor

Overview

The Cortex-M0 processor has an exceptionally small silicon area, low power and minimal code footprint, enabling developers to achieve 32-bit performance at an 8-bit price point, bypassing the step to 16-bit devices. The ultra-low gate count of the processor enables its deployment in analog and mixed signal devices.

Features

Feature	Description
Architecture	Armv6-M
Pipeline	3-stage
Bus Interface	AMBA AHB-Lite (Von Neumann bus architecture)
Interrupts	Non-maskable Interrupt (NMI) and up to 32 physical interrupts
Wake-up Interrupt Controller (WIC)	Optional for waking up the processor from state retention power gating or when all clocks are stopped
Sleep Modes	Integrated Wait For Interrupt (WFI) and Wait For Event (WFE) instructions and Sleep On Exit capability Sleep and Deep Sleep signals Optional retention mode with Arm Power Management Kit
Enhanced Instructions	Hardware single-cycle (32x32) multiply
Debug	Optional JTAG and Serial Wire Debug ports Up to four breakpoints and two watchpoints

About the Processor

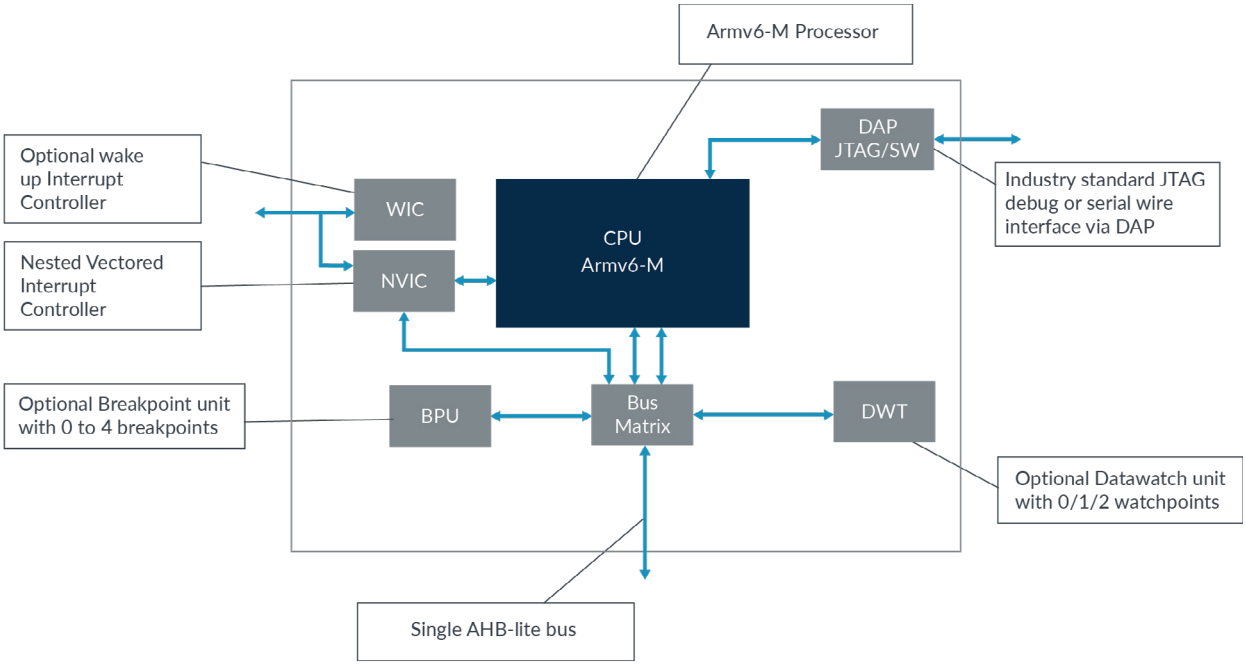
The Cortex-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes a Nested Vectored Interrupt Controller (NVIC) component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processors.

Processor features

- The Armv6-M Thumb® instruction set with Thumb-2 technology
- Optionally, an Armv6-M compliant 24-bit SysTick timer
- A 32-bit hardware multiplier. This can be the standard single-cycle multiplier, or a 32-cycle multiplier that has a lower area and performance implementation
- Support for either little-endian or byte invariant big-endian data accesses
- The ability to have deterministic, fixed-latency, interrupt handling
- Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
- Armv6-M C Application Binary Interface (C-ABI) compliant exception model enabling the use of pure C functions as interrupt handlers
- Low power sleep-mode entry using WFI and WFE instructions, or the return from interrupt sleep-on-exit feature

Block Diagram

Figure 2: Cortex-M0 processor components



Cortex-M0+ Components

NVIC features

- 1, 2, 4, 8, 16, 24, or 32 external interrupt inputs, each with four levels of priority
- Dedicated NMI input
- Support for both level-sensitive and pulse-sensitive interrupt lines
- Optional WIC providing ultra-low power sleep mode support

Optional debug support

- Zero to four hardware breakpoints
- Zero to two watchpoints
- Program Counter Sampling Register (PCSR) for non-intrusive code profiling, if at least one hardware data watchpoint is implemented
- Single step and vector catch capabilities
- Support for unlimited software breakpoints using BKPT instruction
- Non-intrusive access to core peripherals and zero-wait state system slaves through a compact bus matrix. A debugger can access these devices, including memory, even when the processor is running
- Full access to core registers when the processor is halted
- Optional, low gate-count CoreSight compliant debug access through a Debug Access Port (DAP) supporting either Serial Wire or JTAG debug connections

Bus interfaces

- Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
- Single 32-bit slave port that supports the DAP

Interfaces

AHB-Lite interface

Transactions on the AHB-Lite interface are always marked as non-sequential.

Processor accesses and debug accesses share the external interface to external AHB peripherals. The processor accesses take priority over debug accesses.

Any vendor specific components can populate this bus.

Debug Access Port

The processor has a low gate count DAP. This provides a Serial Wire or JTAG debug port and connects to the processor slave port to provide full system-level debug access.

The processor slave port can be configured to connect to a full CoreSight DAP system, with the processor providing full multiprocessor debug simultaneous halt and release cross-triggering capabilities.

Cortex-M0 Pipeline

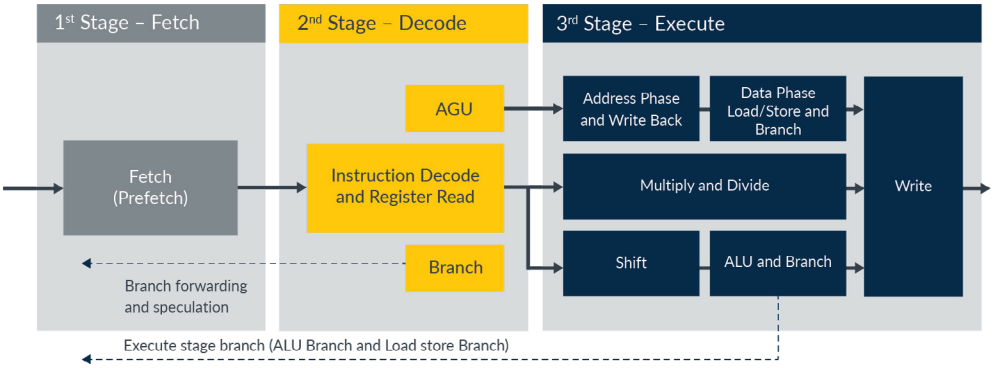


Figure 3: Cortex-M0 processor pipeline

Corstone-101

Corstone-101 is a licensable package that includes many useful components including the Cortex-M System Design Kit (CMSDK) which provides all the fundamental system elements to design an Soc around Arm Cortex-M0.

Features include:

- A selection of AMBA AHB and APB infrastructure components
- Essential peripherals such as GPIO, timers, watchdog, and UART
- Example systems for Cortex-M0, Cortex-M0+, Cortex-M3, and Cortex-M4 processors
- Compilation and simulation scripts for the Verilog environment
- Software driver and example programs

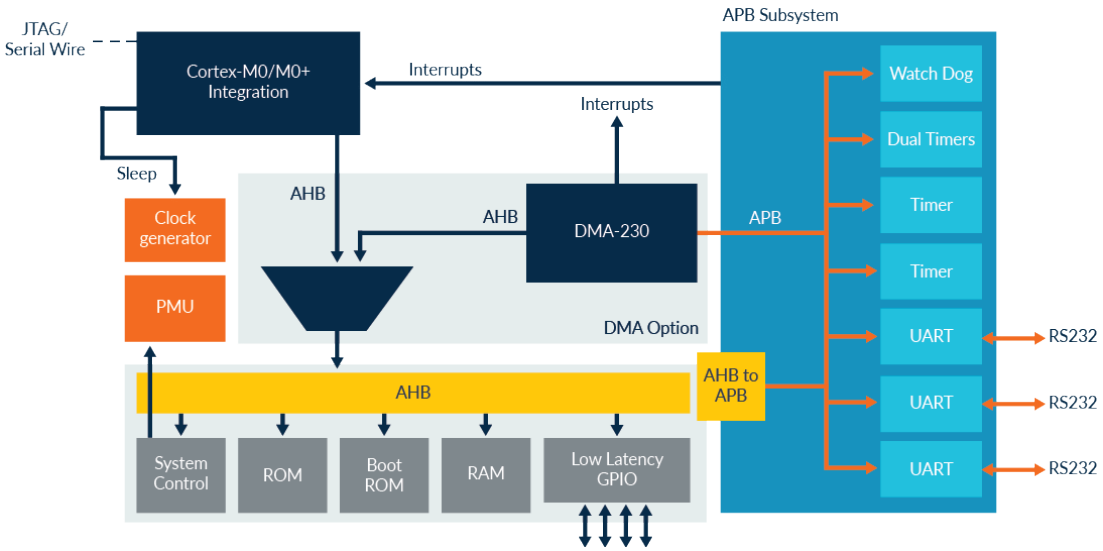


Figure 4: Example System for Cortex-M0

Processor Configuration Options

The Cortex-M0 processor has configurable options that can be set during the implementation and integration stages to match the functional requirements.

Feature	Options
Interrupts	External interrupts 1-32
Data Endianness	Little-endian or big-endian
SysTick Timer	Present or absent
Number of Watchpoint Comparators	0, 1, 2
Number of breakpoint comparators	0, 1, 2, 3, 4
Halting Debug Support	Present or absent
Halting Debug Support	Present or absent
Multiplier	Fast or small

Instruction Set

Figure 5: Instruction set

Power, Performance and Area

DMIPS	CoreMark/MHz
0.87	2.25

Configuration	90LP Arm SC7 RVT SS 1.08V, 125°C		40LP Arm SC9 RVT C50 SS 0.99V, 125°C	
	Area mm²	Power µW/MHz	Area mm²	Power µW/MHz
Minimum Configuration*	0.0303	12.5	0.0073	5.1
Typical**	0.0604	16.6	0.0155	6.7

Max Freq	90LP Arm SC7 RVT SS 1.08V, 125°C	40LP Arm SC9 RVT C50 SS 0.99V, 125°C
Typical**	268MHz	280MHz

* 1 IRQ, small multiplier, no debug, no WIC, 2 WIC lines 0 breakpoints, 0 watchpoints

** 32 IRQ, fast multiplier, Debug, SysTick timer & WIC present, 34 WIC lines 4 breakpoints, 2 watchpoints

Additional Technical Documents

1. Cortex-M0 Technical Reference Manual - TRM
2. Cortex-M0 Integration and Implementation Manual – available as part of the Bill of Materials
3. Armv6-M Architecture Reference Manual - ARM
4. CoreSight MTB-M0 Technical Reference Manual - MTB

Glossary of Terms

AHB-Lite	Advanced High-performance Bus Lite
BPU	Breakpoint Unit
C-ABI	C Application Binary Interface
DWT	Data Watchpoint and Trace
JTAG	Joint Test Action Group
NMI	Non-maskable Interrupt
NVIC	Nested Vectored Interrupt Controller
SWO	Serial Wire Output
WFE	Wait for Event
WFI	Wait for Interrupt
WIC	Wake-up Interrupt Controller

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